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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,399	09/18/2003	Michael S. Leung	P0298US-7	8955
7590	09/30/2005		EXAMINER	
Jaye G. Heybl KOPPEL, JACOBS, PATRICK & HEYBL Suite 107 555 St. Charles Drive Thousand Oaks, CA 91360			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	
			DATE MAILED: 09/30/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/666,399	MICHAEL LEUNG
	Examiner Thao X. Le	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 August 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) 1-12 and 20-32 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 13-19 and 33-37 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6376277 to Corisis.

Regarding claim 13, Corisis discloses a method for coating a plurality of semiconductor device, comprising: providing a mold, column 4 line 44, with a formation cavity 75, column 4 line 46, for holding a plurality of semiconductor devices 20, fig. 6A, said formation cavity 75 at least partially defined by upper 70 and lower 72, column 4 line 52, mounting a plurality of semiconductor devices 20, fig. 6A, within said mold formation cavity 75; injecting or otherwise introducing curable coating material 40, column 4 lines 40 and 55, into said mold to fill said mold formation cavity 75 and at least partially cover said semiconductor devices 20 with coating material 40; and curing, or otherwise treating said coating material, column 4 line 55, so that said semiconductor devices 20 are at least partially embedded in said cured coating material 40, fig. 6A.

Regarding claims 14-15, Corisis discloses the method further comprising removing said cured or treated coating material 40 with said embedded semiconductor devices 20 from said formation cavity 75, further comprising separating said embedded

semiconductor devices 20 so that each is at least partially covered by a layer of said cured or treated coating material 20, column 5 lines 1-3.

Regarding claim 16, Corisis discloses the method wherein upper and lower sections 70/72 provide opposing parallel surface, said semiconductor devices 6A arranged on one or both of said opposing surfaces, fig. 6A.

Regarding claim 17, Corisis discloses the method claim wherein said curing otherwise treating said semiconductor material comprises one of the methods from the group comprising heat curing, optical curing or room temperature curing, column 4 line 56.

Regarding claim 18, Corisis discloses a method wherein the semiconductor devices 20 are separated by dicing or scribe and break, column 5 line 2.

Regarding claim 19, Corisis discloses the method wherein the semiconductor devices are separated such that the layer of cured or otherwise treated coating material 40 conforms to the shape of the semiconductor device 20, fig. 6A.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 33-34, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6376277 to Corisis.

Regarding claims 33-34, 36-37, as discussed in the claims 13-19 above Corisis discloses all the limitations of claim 33 except the plurality of LEDs.

At the time the invention was made; it would have been obvious to one of ordinary skill in the art to replace the semiconductor die 20 of Corisis with the LEDs for intended purposes, MPEP 2144.07. Furthermore, such semiconductor die or LED packaging is typical in the art as disclosed by Chen in fig. 20.

6. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6376277 to Corisis in view of US 6252254 to Soules et al.

Regarding claim 35, Corisis does not disclose the method wherein the matrix material 5 contains light conversion particles.

However, Soules discloses the method wherein the LED, fig. 2, comprises a matrix material 15 contains light conversion particles, column 6 lines 15-25. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the encapsulating material contains light conversion

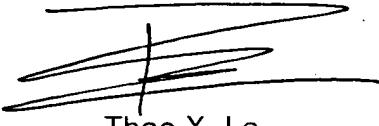
particles teaching of Soules with Corisis's capsulation material 40, because it would have created a specific LED characteristics such as color and color rendering index, as taught by Soules, column 2 line 27-32.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
25 Sept. 2005